UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/790,983	03/01/2004	Nathan Zommer	011775-010210US	1309

20350 7590 09/24/2004

TOWNSEND AND TOWNSEND AND CREW, LLP
TWO EMBARCADERO CENTER
EIGHTH FLOOR
SAN FRANCISCO, CA 94111-3834

EXAMINER	
LOKE, STEVEN HO YIN	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 09/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/790,983	ZOMMER ET AL.	
	Examiner	Art Unit	
	Steven Loke	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-13 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-13 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

2. The abstract of the disclosure is objected to because the abstract should disclose the method to make the power device. Correction is required.

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1, 2, 6, 7 and 9-12 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Dupuy et al.

In regards to claim 1, Dupuy et al. inherently show a method for manufacturing a semiconductor power device in figs. 10 and 11. It comprising: identifying an active region on a semiconductor die [35]; identifying a first region [121] in said active region; identifying a second region [122-125] in said active region; providing a first cell design by which active cells in said first region will be fabricated (the transistors [111] are fabricated with short distance [117] between the source regions [114]); and providing a second cell design by which active cells in said second region will be fabricated (the transistors [112] are fabricated with long distance [116] between the source regions [114]), said first cell design being different from said second cell design.

In regards to claim 2, Dupuy et al. further disclose said first cell design and said second cell design include cell dimensions such that a cell density of said first region is different from that of said second region (there are more transistors [112] in the second region [122-125] than the first region [121]).

In regards to claim 7, Dupuy et al. further disclose said first cell design differs from said second cell design with respect to current density (col. 6, line 65 to col. 7, line 15).

In regards to claim 9, Dupuy et al. inherently disclose said first cell design differs from said second cell design with respect to transconductance because the current density of the first cells is different than that of the second cells.

In regards to claim 10, Dupuy et al. inherently disclose said first cell design differs from said second cell design with respect to gain because the current density of the first cells is different than that of the second cells.

In regards to claim 12, Dupuy et al. disclose said first cell design and said second cell design are field effect transistors.

In regards to claim 6, Dupuy et al. inherently show a method for manufacturing a semiconductor power device in fig. 9. It comprising: identifying an active region on a semiconductor die; identifying a first region [101] in said active region; identifying a second region [102-105] in said active region; providing a first cell design by which active cells in said first region will be fabricated (the transistors [111] are doped with p-type dopant to increase the threshold voltage of the transistors); and providing a second cell design by which active cells in said second region will be fabricated (the transistors without an additional p-type dopant), said first cell design being different from said

second cell design; said first cell design includes a material composition (p-type dopant) for cells that is different from that of said second cell design.

In regards to claim 11, Dupuy et al. disclose said first cell design differs from said second cell design with respect to threshold voltage.

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1, 3-5 and 8 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Tsunoda et al.

In regards to claim 1, Tsunoda et al. inherently show a method for manufacturing a semiconductor power device in figs. 3A-10. It comprising: identifying an active region on a semiconductor die; identifying a first region [21] in said active region; identifying a second region [22] in said active region; providing a first cell design by which active cells in said first region will be fabricated (the transistors have a larger channel width y); and providing a second cell design by which active cells in said second region will be fabricated (the transistors have a smaller channel width x), said first cell design being different from said second cell design.

In regards to claim 3, Tsunoda et al. further disclose said first cell design includes at least one physical dimension different from that included in said second cell design (the channel width (x, y) and the base regions [14a, 14b] and the insulated gate [13]).

In regards to claim 4, Tsunoda et al. further disclose said physical dimension includes a channel width (x, y).

In regards to claim 5, Tsunoda et al. further disclose said physical dimension includes a cell die area (base regions [14a, 14b] and the insulated gate [13]).

In regards to claim 8, Tsunoda et al. inherently disclose said first cell design differs from said second cell design with respect to source resistance because the emitter (source) [15] in base [14b] is larger than the emitter (source) [15] in base [14a].

7. Claims 1 and 13 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Shukuri et al.

In regards to claim 1, Shukuri et al. show a method for manufacturing a semiconductor power device (the memory transistors are considered as power devices because they dissipate thermal energy) in figs. 1-34. It comprising: identifying an active region on a semiconductor die [120]; identifying a first region (the region occupied by the transistors for DRAM [106] and flash memories [113-115]) in said active region; identifying a second region (the region occupied by the transistors for cache memory [108]) in said active region; providing a first cell design by which active cells in said first region will be fabricated (the transistors having thick gate oxides); and providing a second cell design by which active cells in said second region will be fabricated (the transistors having thin gate oxides), said first cell design being different from said second cell design.

In regards to claim 13, Shukuri et al. further show the said first cell design and said second cell design are memory cells.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven Loke whose telephone number is (571) 272-1657. The examiner can normally be reached on 7:50 am to 5:20 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

sl
September 19, 2004

Steven Loke
Primary Examiner